

# AHMAD KARIMI

Ajax, ON L1Z1J7

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## Education

Lassonde School of Engineering, York University

Sep. 2022 – May 2027

Bachelor of Engineering (BEng) Computer Engineering

Toronto, ON

## Relevant Coursework

- Data Structures
- Algorithms
- Operating Systems
- Computer Architecture
- Embedded Systems
- Computer Networks
- Applied Linear Algebra
- Engineering Statistics

## Projects

Natural Language Communicator | AWS, Docker, Terraform, PostgreSQL, Ollama, Redis

July 2025

- Architected and deployed a scalable cloud platform enabling policy analysts to interact with large language models.
- Engineered a Docker-based microservices architecture supporting backend APIs and frontend integration.
- Deployed Ollama inference on AWS EC2, enabling scalable model inference beyond local hardware limitations.
- Reduced average response latency by 30–40% through Redis-based response caching.
- Reduced AWS compute costs by 20% through optimized instance configuration and batching.

FPGA Bluetooth-Controlled “Dino Runner” Game | Verilog, DE10-Lite, VGA, UART, Quartus

December 2025

- Built a complete FPGA game system integrating VGA rendering, FSM-based gameplay, Bluetooth UART input, and 7-segment scoring in modular Verilog.
- Developed 640×480 @ 60Hz VGA graphics pipeline with real-time obstacle motion and hitbox-based collision detection.
- Designed and validated a UART receiver with oversampling ticks and mid-bit sampling FSM, generating a clean jump pulse via 2-FF synchronization and rising-edge detection.
- Leveraged LFSR-based randomness for obstacle spawn timing (3 obstacle slots) and randomized LED death patterns.
- Engineered time-based scoring with persistent high score (switch-selectable) and LFSR-driven player color toggling.

32-Bit Pipelined CPU Design | Verilog, ModelSim, FPGA (DE10-Lite)

October 2024

- Designed a 32-bit pipelined CPU in Verilog implementing fetch, decode, execute, and memory stages.
- Built modular ALU, register file, and control logic components to support arithmetic and logical instructions.
- Developed ripple-carry adders and multiplexers to enable arithmetic operations and instruction selection logic.
- Implemented branch and jump handling logic to support control-flow instruction execution within the datapath.
- Verified functionality across 100+ simulation test cases covering arithmetic, logical, branch, and memory operations.
- Achieved stable timing closure at 50 MHz on DE10-Lite FPGA through full hardware synthesis and validation.

## Experience

Reliance Home Comfort

May 2023 – Present

Inventory Clerk (Co-op & Part-Time)

Whitby, ON

- Reorganized and tracked \$7,000+ in tools/parts, improving accuracy and saving the branch significant costs.
- Used CRM and Excel for inventory, reporting, and process optimization, strengthening technical and analytical skills.
- Collaborated with teams and trained new employees, ensuring smooth operations and alignment with contractors.
- Retained part-time after co-op for reliability and leadership in driving process improvements.

## Technical Skills

Languages: Python, Java, C++, Verilog, JavaScript, SQL

Frameworks & Tools: React, FastAPI, Docker, Terraform, PostgreSQL, Git

Cloud DevOps: AWS (EC2, S3, IAM), CI/CD (GitHub Actions)

## Leadership / Extracurricular

EDGE York

September 2022 – 2024

Executive Member

York University

- Organized and promoted campus-wide professional development events supporting marginalized students.
- Coordinated with corporate partners and student leaders to execute speaker panels and networking sessions.
- Contributed to strategic planning and recruitment initiatives to expand campus engagement.
- Supported outreach efforts increasing student participation and event attendance.